GBGS Scheme

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Third Semester B.E. Degree Examination, June/July 2018 Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

- 1 What is MOSFET? Name its types. Explain the construction of n-channel E-MOSFET.
 - Compare JFET and MOSFET.

(06 Marks) (05 Marks)

Explain self-bias circuit for JFET.

(05 Marks)

OR

Define (i) CMRR ii) Slew rate iii) PSRR iv) Bandwidth pertaining to OPAMP.

(06 Marks)

- Explain with schematics operation of relaxation oscillator with relevant waveforms.
 - What are active filters? Explain active low pass filter.

(05 Marks)

(05 Marks)

Module-2

3 Using Q-M method, simplify the expression $f(A, B, C, D) = \Sigma(0, 3, 5, 6, 7, 11, 14)$.

(06 Marks)

- Explain about positive and negative logic prove that positive 'OR' is equal to negative 'AND'. (05 Marks)
- What are Hazards? Briefly describe about designing Hazard free circuit.

(05 Marks)

OR

Give Sum-Of-Product (SOP) and Product-Of-Sum (POS) circuit for

 $f(A, B, C, D) = \sum m (6, 8, 9, 10, 11, 12, 13, 14, 15).$

(06 Marks)

b. Explain the verilog program structure.

(05 Marks)

Design a logic circuit to provide an output when any two or three of four switches are closed. (05 Marks)

Module-3

- Implement the following Boolean function using 4:1 multiplexer $F(A, B, C, D) = \sum m (0, 1, 1)$ 5 2, 4, 6, 9, 12, 14). (06 Marks)
 - b. Construct 16:1 multiplexer using 4:1 and 2:1 multiplexer.

(05 Marks)

What is a decoder? Give the circuit for 3:8 decoder.

(05 Marks)

- 6 What is a magnitude comparator? Explain a 1-bit comparator with truth table and circuit diagram. (06 Marks)
 - Briefly explain about parity generators and checkers. For a 3 bit message, give the b. expression for even parity bit. (05 Marks)
 - Compare and contrast PLA and PAL.

(05 Marks)

Module-4

- Explain the working of JK master slave flip-flop with a sketch, truth table and symbol.
 - (06 Mark -

Give a brief account an flip flop as finite state machine.

(05 Mark -)

Briefly describe about sequential logic circuit.

(05 Mark -

OR

Enumerate different types of shift registers. Explain Serial In Serial Out (SISO) register 8

(06 Marks)

Mention the applicators of shift registers.

(05 Mark s

Using behavioral model write verilog HDL code for a 'D' flipflop with reset input.

(05 Marks

Module-5

Explain digital clock with block diagram.

(06 Marks)

Design a 3 bit synchronous binary counter using JK flip flop.

(05 Marks)

Mention different types of A/D converters and test its specifications.

(05 Mark 81

OR

Explain binary weighted resistor D/A converter. Mention its drawbacks. **10** a.

(06 Marks)

Describe about successive approximation type ADC.

(05 Marks)

What is the resolution of a 12 bit D/A converter which uses a binary ladder, if the full scale (05 Marks) output is +10V?